FIG.1

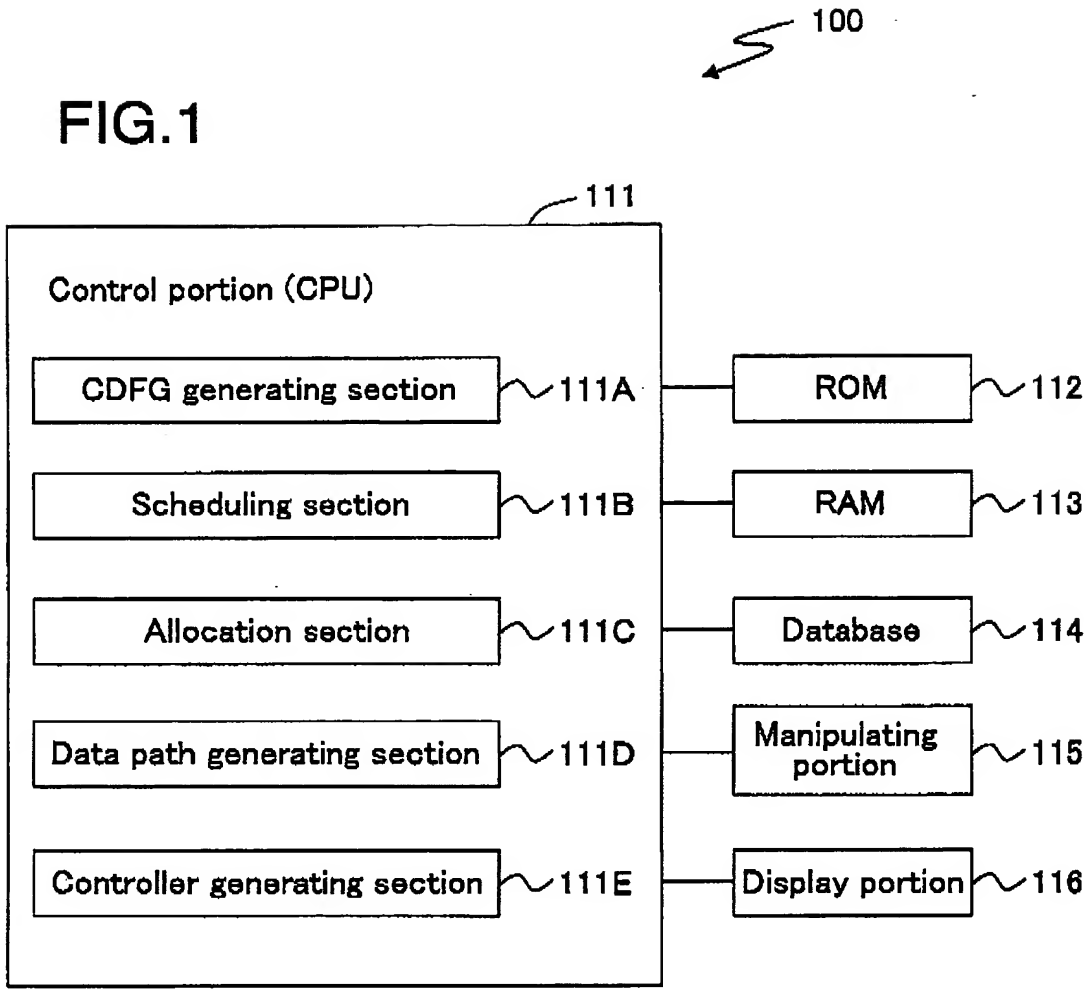

100
111
Control portion (CPU)
CDFG generating section
111A
Scheduling section
111B
Allocation section
111C
Data path generating section
111D
Controller generating section
111E
ROM
112
RAM
113
Database
114
Manipulating portion
115
Display portion
116

FIG.2

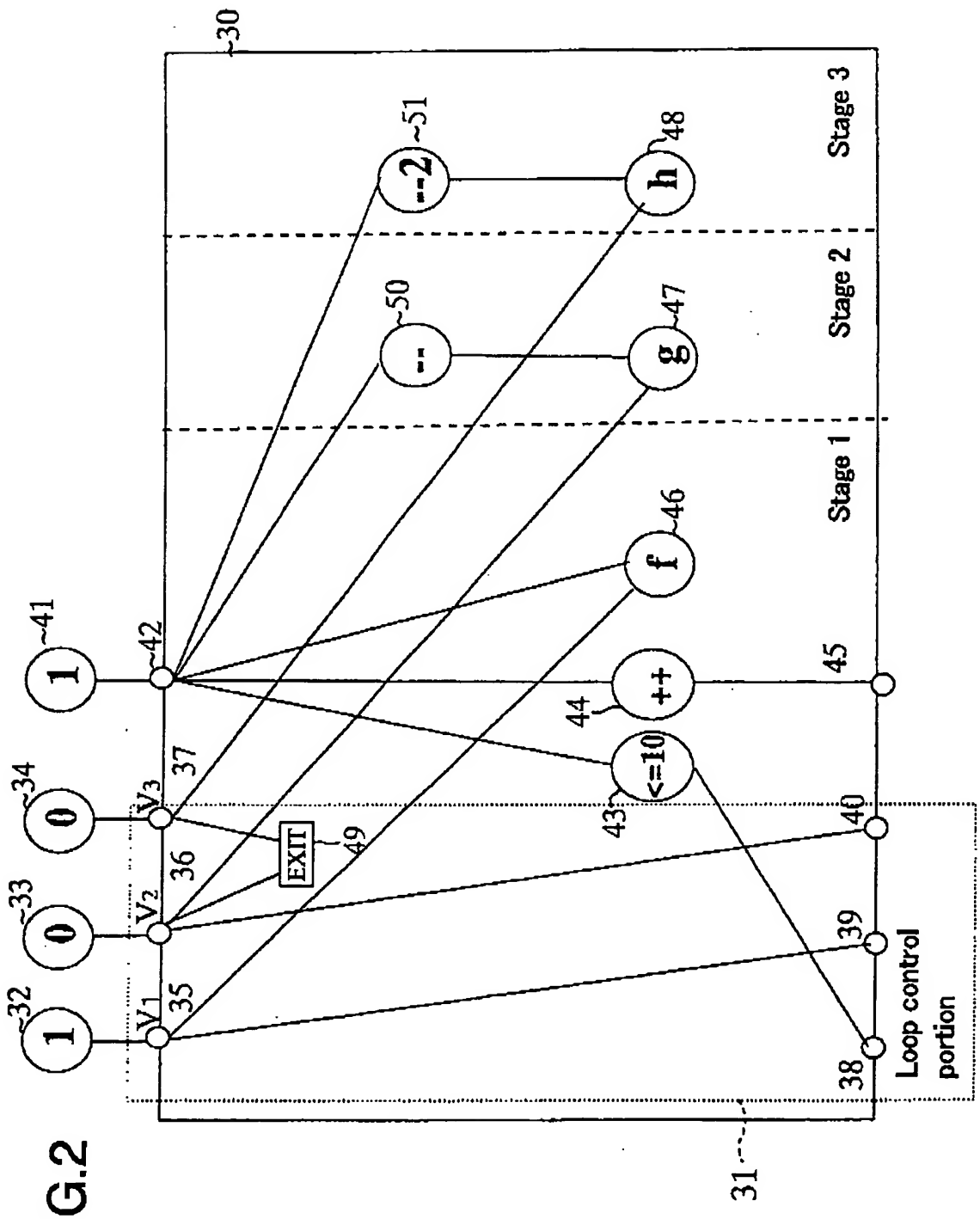

30
31
32
33
34
41
42
35
36
37
38
39
40
43
44
45
46
47
48
49
50
51
1
0
0
1
V1
V2
V3
EXIT
f
g
h
++
--
--2
<=10
Stage 1
Stage 2
Stage 3
Loop control portion

FIG.3

Cycle	V1	V2	V3
1	1	0	0
2	1	1	0
3～10	1	1	1
11	0	1	1
12	0	0	1

FIG.4

Cycle	V1	V2	V3
1	1	0	0
2	0	1	0
3	0	0	1

FIG.5

```
j = 5;
for (i = 0; i<10 ; i++)
{
   a[i] = i ;
   j += i ;
   b[i] = j ;
}
```

FIG.6

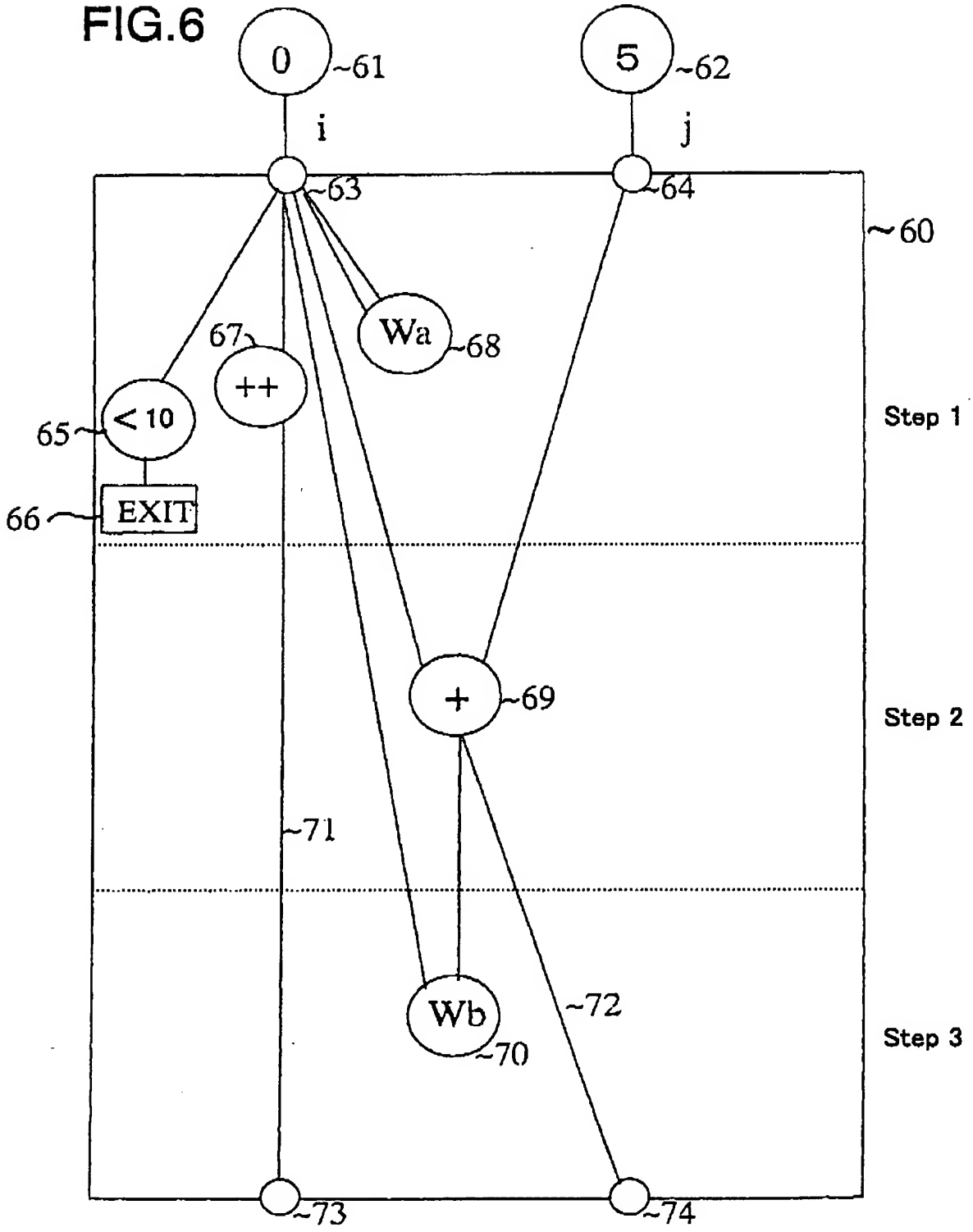

0
~61
5
~62
i
j
~63
~64
~60
67
++
Wa
~68
65
< 10
66
EXIT
Step 1
+
~69
Step 2
~71
Wb
~70
~72
Step 3
~73
~74

FIG.7

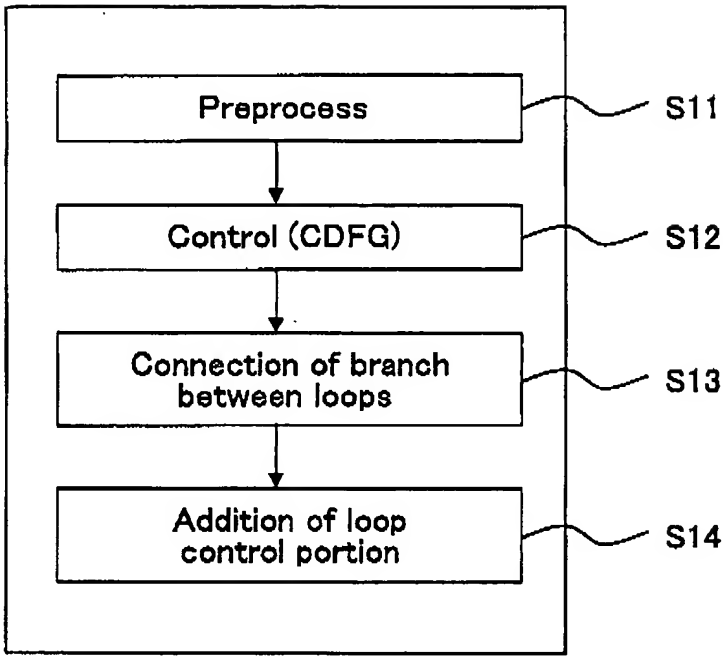

Preprocess
S11
Control (CDFG)
S12
Connection of branch between loops
S13
Addition of loop control portion
S14

FIG.8A

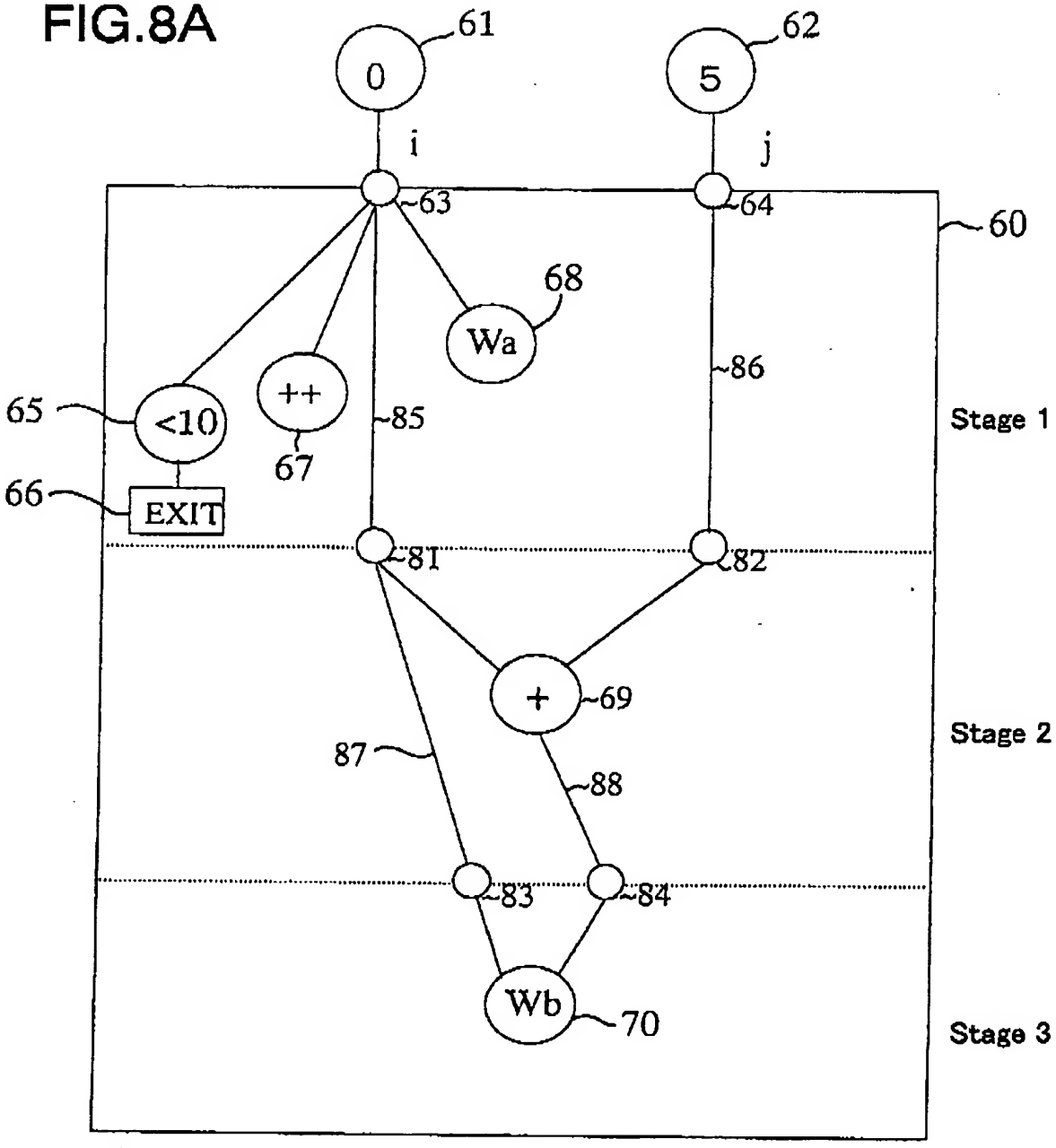

0
61
5
62
i
j
63
64
60
68
Wa
86
65
<10
++
85
Stage 1
67
66
EXIT
81
82
+
69
Stage 2
87
88
83
84
Wb
70
Stage 3

FIG.8B

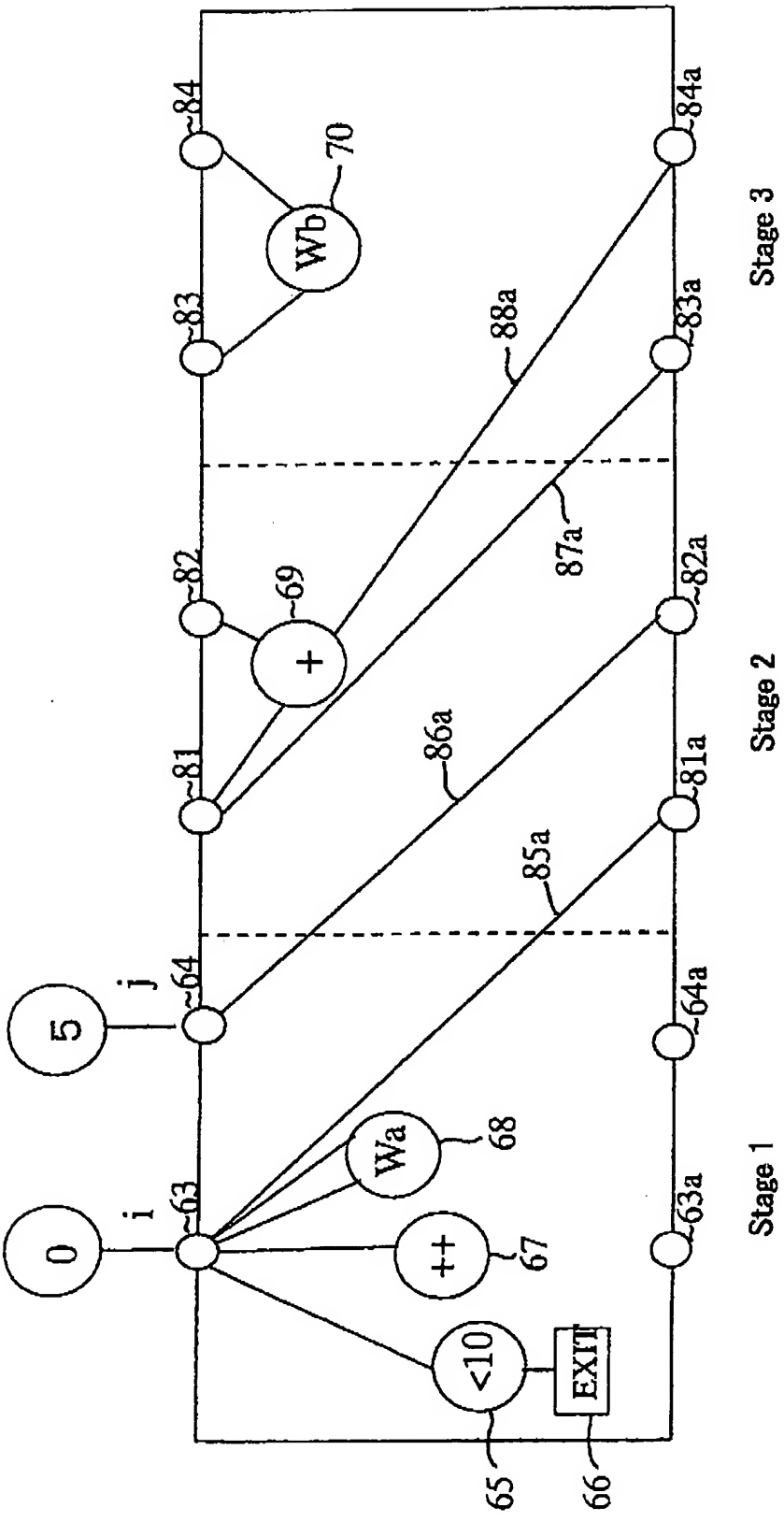

0
i
5
j
63
64
Wa
68
++
67
<10
65
EXIT
66
63a
64a
81
81a
82
82a
+
69
83
83a
Wb
70
84
84a
85a
86a
87a
88a
Stage 1
Stage 2
Stage 3

FIG.8C

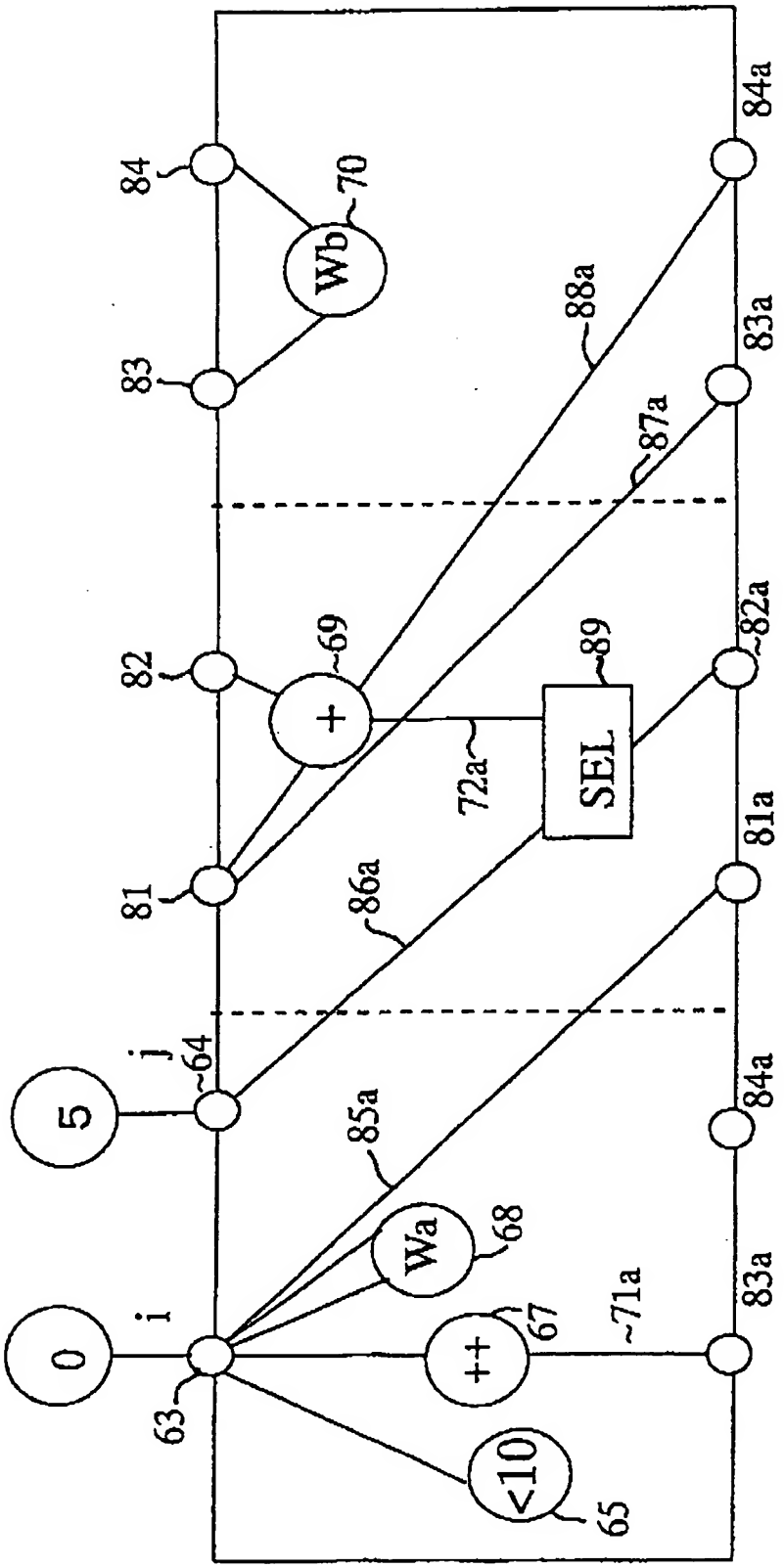

0
i
63
5
j
64
Wa
68
++
67
<10
65
71a
85a
86a
72a
SEL
89
+
69
Wb
70
81
82
83
84
87a
88a
81a
82a
83a
84a
83a
84a

FIG.8D

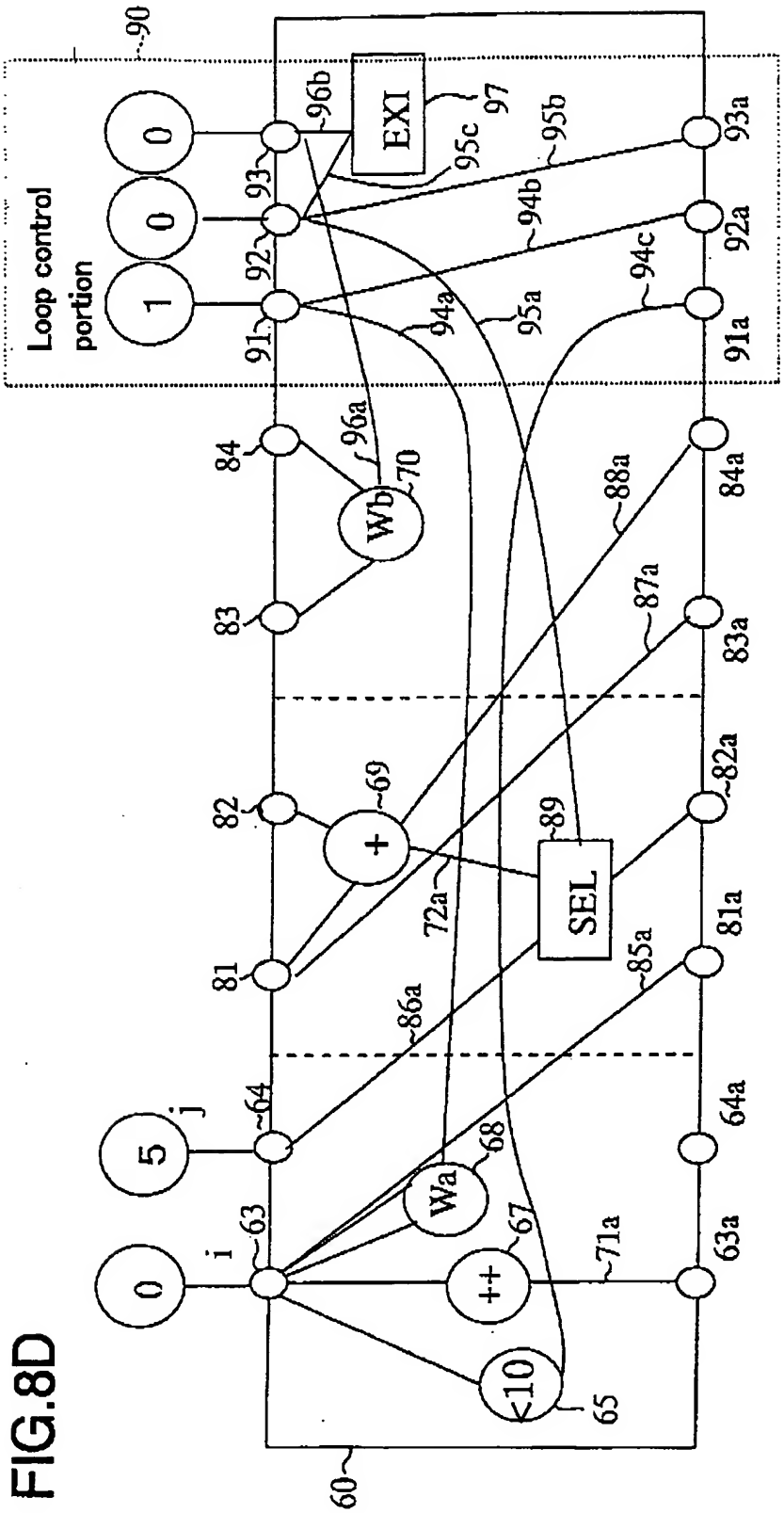

Loop control portion
90
0
0
1
91
92
93
EXI
97
96b
95c
95b
94b
94c
94a
95a
93a
92a
91a
84
96a
Wb
70
83
88a
84a
87a
83a
82
69
+
89
SEL
72a
82a
81
81a
85a
86a
64
5
j
64a
Wa
68
0
i
63
67
++
71a
63a
10
65
60

FIG.9

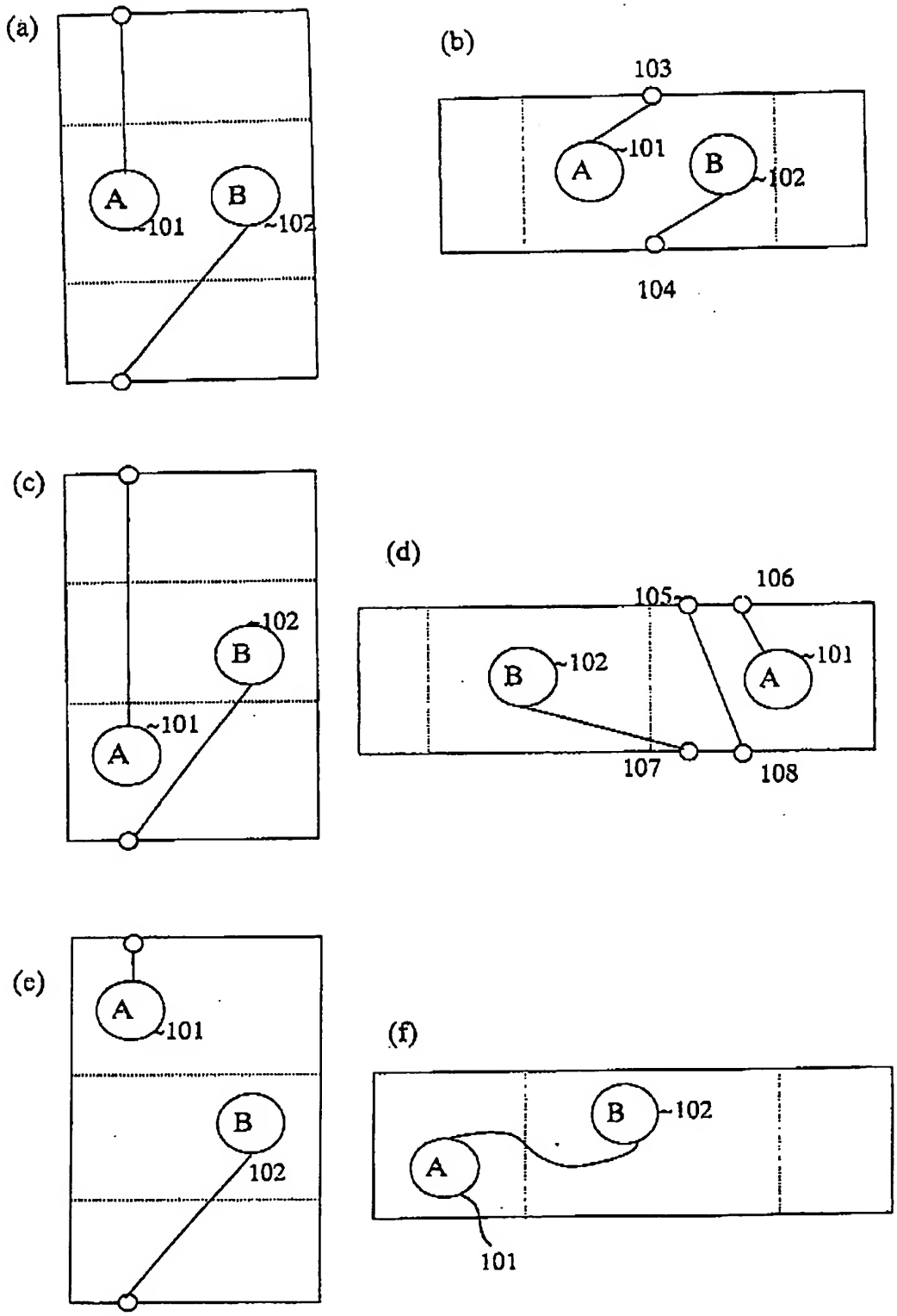

(a)
A
101
B
102
(b)
103
A
101
B
102
104
(c)
102
B
101
A
(d)
105
106
B
102
A
101
107
108
(e)
A
101
B
102
(f)
B
102
A
101

FIG.10

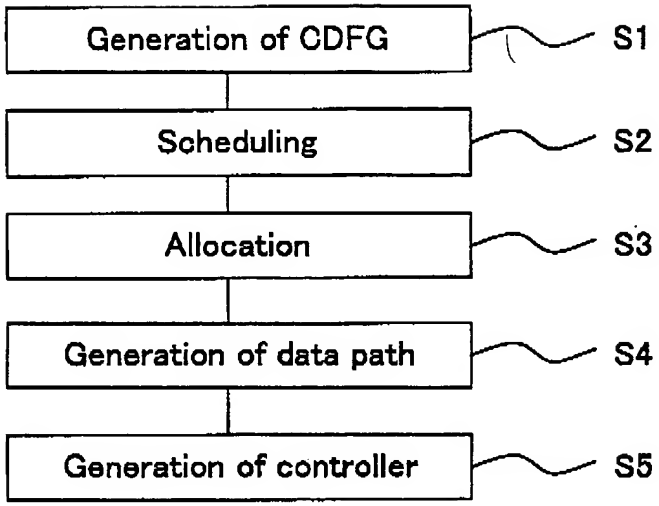


FIG.11

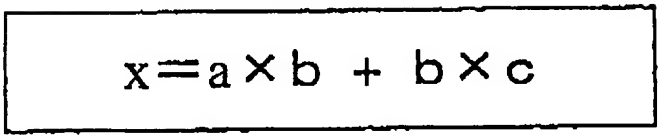


FIG.12

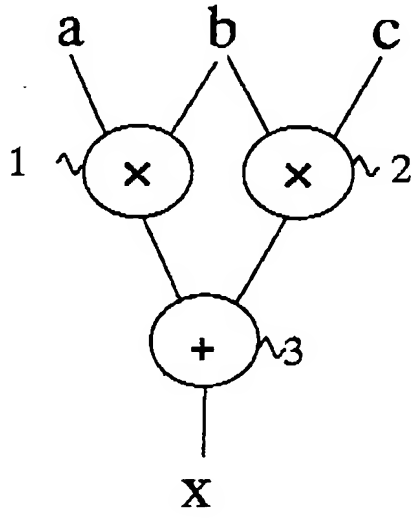


FIG.13

```
struct Node
  {
   int   node_id;
   int   in_edge[2];
   int   out_edge[1];
   int   op_type;
   }
struct Edge
  {
   int   edge_id;
   int   from_node;
   int   to_node;
   }
```

FIG.14

```
for( i =0; i <=10 ; i++)
{
    f(i);
    g(i);
    h(i);
}
```

FIG.15

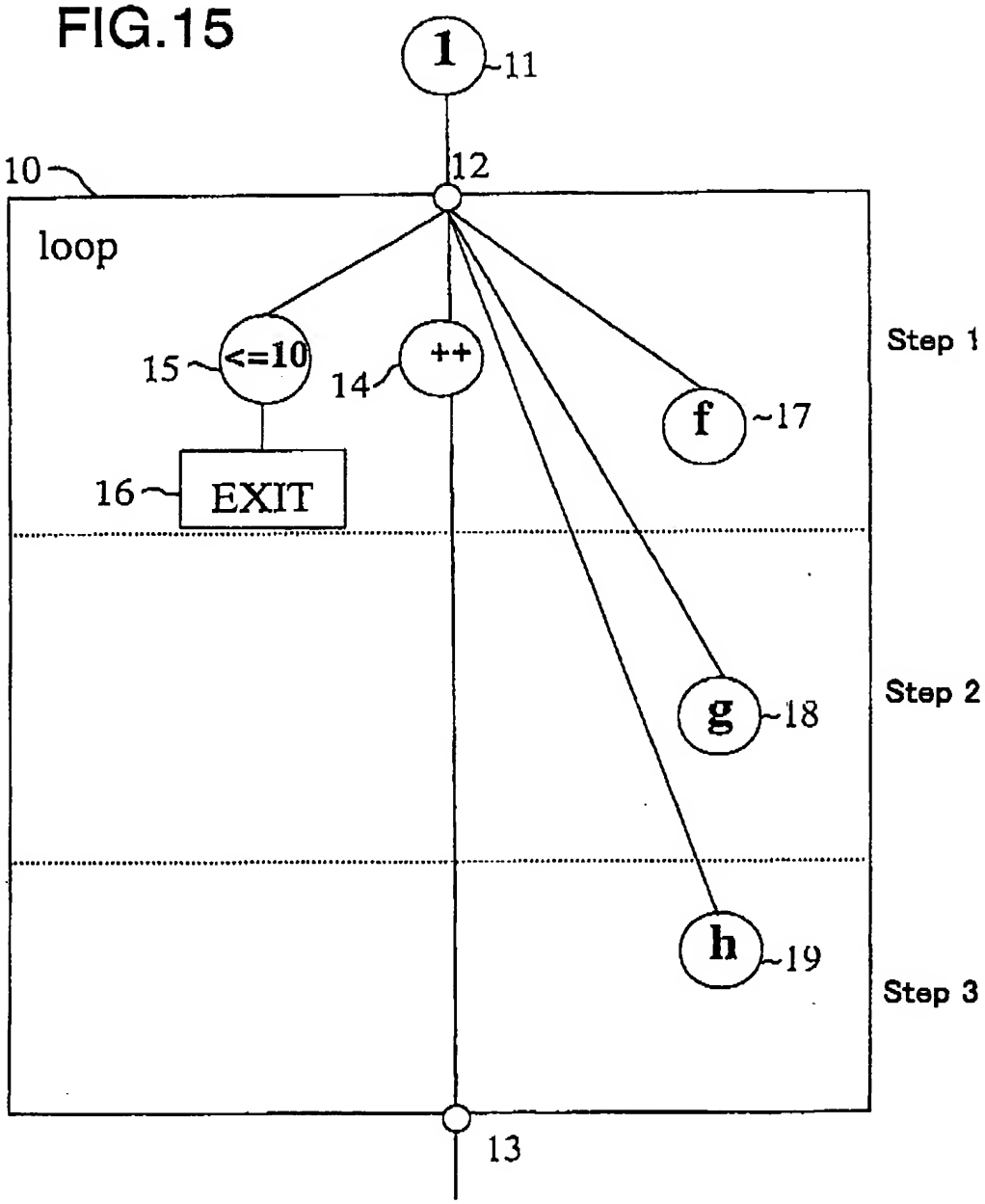


FIG.16

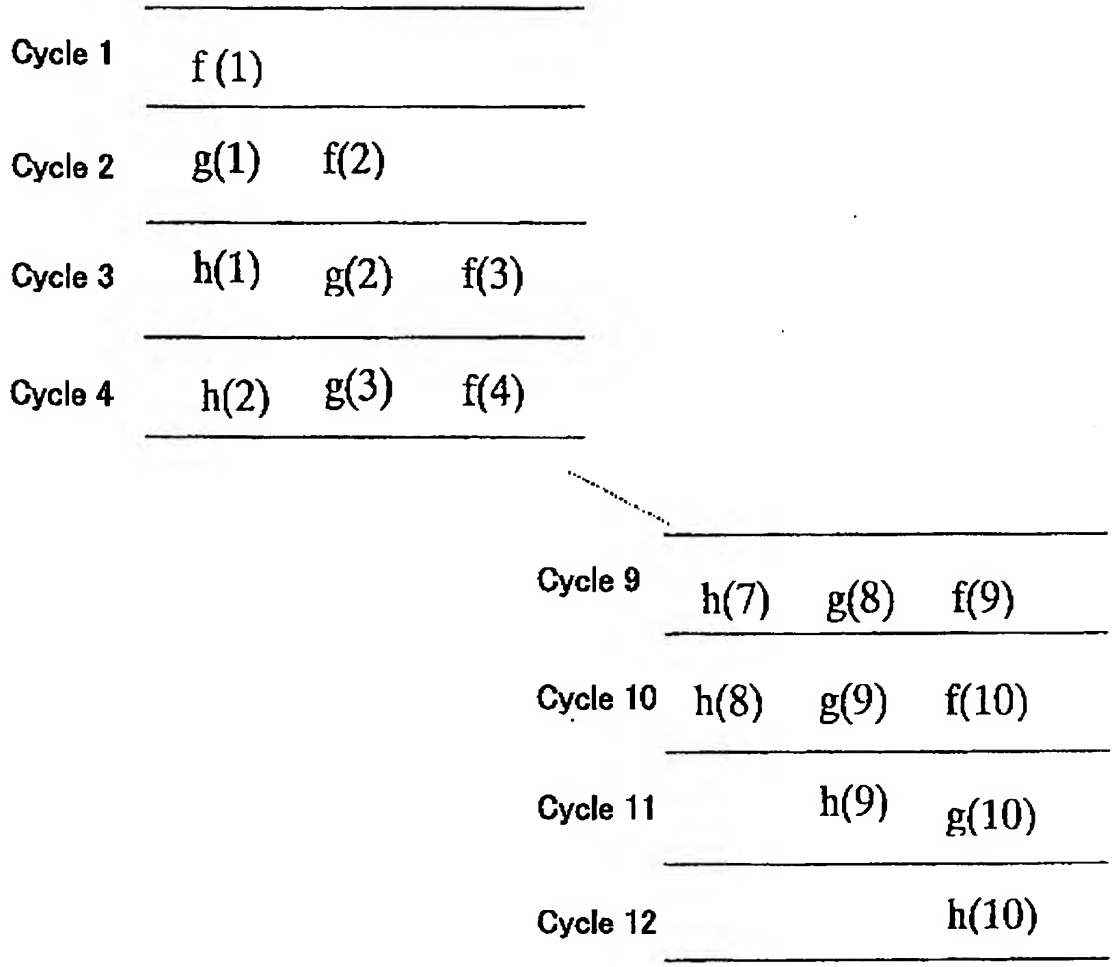
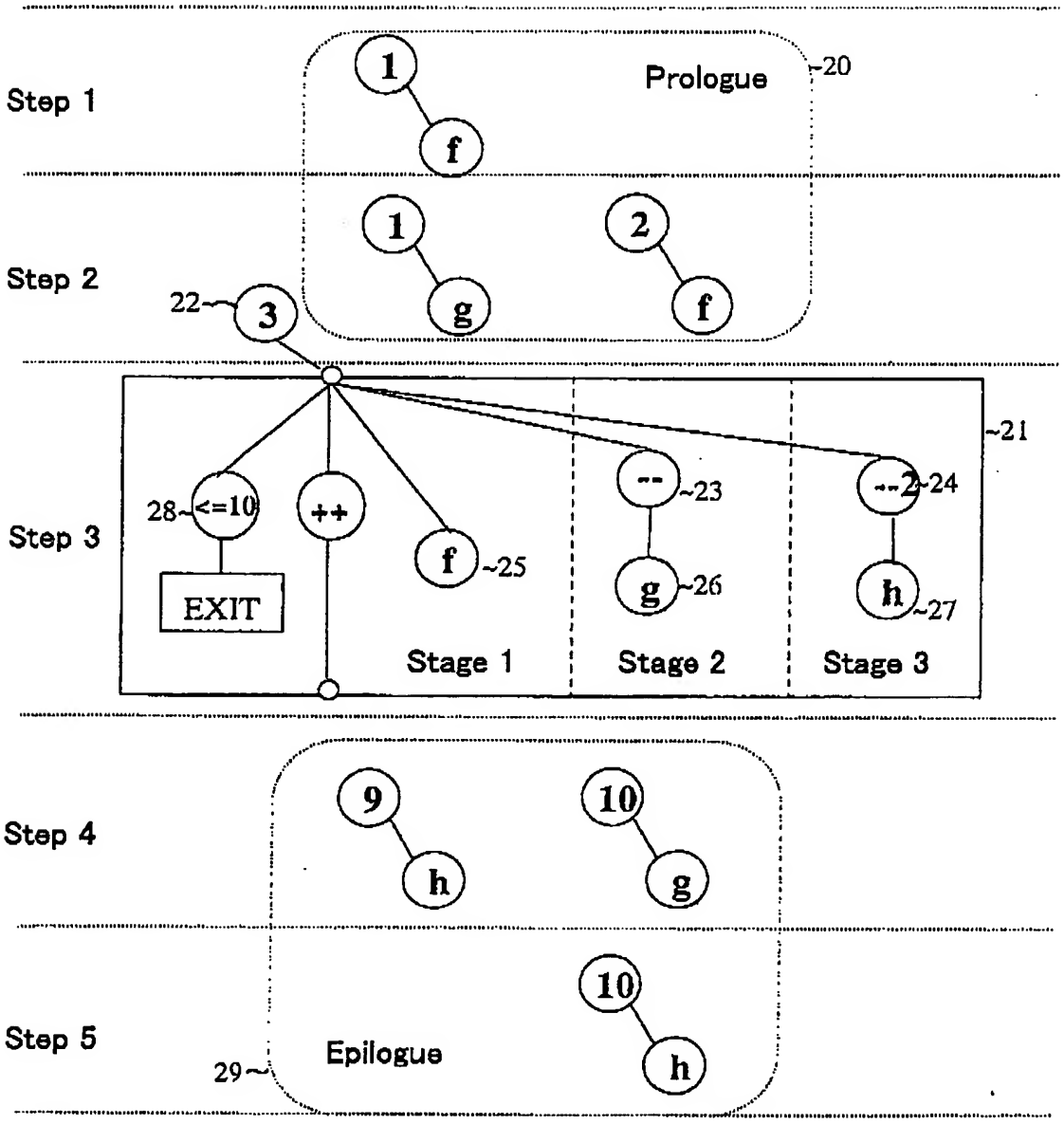

Cycle 1
f (1)
Cycle 2
g(1) f(2)
Cycle 3
h(1) g(2) f(3)
Cycle 4
h(2) g(3) f(4)
Cycle 9
h(7) g(8) f(9)
Cycle 10
h(8) g(9) f(10)
Cycle 11
h(9) g(10)
Cycle 12
h(10)

FIG.17


Step 1
1
f
Prologue
~20
Step 2
1
g
2
f
22~
3
Step 3
~21
28~
<=10
++
f
~25
--
~23
--
~24
EXIT
g
~26
h
~27
Stage 1
Stage 2
Stage 3
Step 4
9
h
10
g
Step 5
10
h
29~
Epilogue